EXHIBIT 9

Express Mail No.:	EV023687891 US
Mailed:	January 21, 2005
Applicant:	James A. Cooper, et al.
Invention:	Optimized Vertical Power DMOSFETS in Silicon Carbide
Serial No.:	Unknown
Filed:	Herewithin
Docket:	64281.P1.US

X Provisional Application Transmittal
X Provisional Application (7 pages)

The stamp of the Patent Office hereon shows receipt of the indicated papers.

CAH

PTO/SB/16 (08-03)
Approved for use through 07/31/2006. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

PROVISIONAL APPLICATION FOR PATENT COVER SHEET

This is a request for filing a PROVISIONAL APPLICATION FOR PATENT under 37 CFR 1.53(c).

Express Mail Label No. **EV 023687891 US**

INVENTOR(S)		
Given Name (first and middle [if any])	Family Name or Surname	Residence (City and either State or Foreign Country)
James Albert	Cooper, Jr.	West Lafayette, Indiana
Asmita	Saha	West Lafayette, Indiana

Additional inventors are being named on the 0 *separately numbered sheets attached hereto*

TITLE OF THE INVENTION (500 characters max)

Optimized Vertical Power DMOSFETS in Silicon Carbide

Direct all correspondence to: **CORRESPONDENCE ADDRESS**

XX Customer Number: 39499

OR

Office of Technology Commercialization
3000 Kent Avenue
West Lafayette, IN 47906-1075

Firm or Individual Name	Purdue Research Foundation				
Address	3000 Kent Avenue				
Address					
City	West Lafayette	State	IN	Zip	47906-1075
Country	USA	Telephone	765-494-2610	Fax	765-496-1277

ENCLOSED APPLICATION PARTS *(check all that apply)*

Specification *Number of Pages* 7 CD(s), Number _____

Drawing(s) *Number of Sheets* 0 Other (specify) _____

Application Date Sheet. See 37 CFR 1.76

METHOD OF PAYMENT OF FILING FEES FOR THIS PROVISIONAL APPLICATION FOR PATENT

Applicant claims small entity status. See 37 CFR 1.27.

FILING FEE
Amount $ 100.00

_____A check or money order is enclosed to cover the filing fees.

__X__The Director is herby authorized to charge filing fees or credit any overpayment to Deposit Account Number: 502939

_____Payment by credit card. Form PTO-2038 is attached.

The invention was made by an agency of the United States Government or under a contract with an agency of the United States Government.

__X__ No.

_____ Yes, the name of the U.S. Government agency and the Government contract number are:

_____

[Page 1 of 1]

Respectfully submitted, Date January 21, 2005

SIGNATURE James A. Cooper REGISTRATION NO. _____ *(if appropriate)*

TYPED or PRINTED NAME James A. Cooper, Jr. Docket Number: 64281.P1.US

TELEPHONE 765-496-7712

USE ONLY FOR FILING A PROVISIONAL APPLICATION FOR PATENT

This collection of information is required by 37 CFR 1.51. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 8 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Mail Stop Provisional Application, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

OFFICE OF TECHNOLOGY COMMERCIALIZATION
DIVISION OF RESEARCH & SCHOLARLY ACTIVITIES
PURDUE RESEARCH FOUNDATION - PURDUE UNIVERSITY 64281

INVENTION RECORD AND DISCLOSURE

CONFIDENTIAL

NOTE: This form requires the signatures of: Department Head(s) and School Dean(s). Please complete the attached form and then route to Department Head(s), Dean(s) and then back to the Office of Technology Commercialization (OTC), 1291 Cumberland Avenue, Suite F, West Lafayette, IN 47906 (Note: Please feel free to add additional attachments to elaborate on any questions, or to call the Office of Technology Commercialization at 42610 for assistance).

I. Formal Record of Disclosure

Please identify by name, phone number, department and building, each individual who contributed to development of the proposed invention *and* who will share in any net proceeds from the proposed invention. Please note that individuals listed here *may or may not* qualify as legal inventors for patent applications. Type the name and campus address of your department (school) head and school dean and *obtain signatures.*

A. **Disclosure Title:** OPTIMIZED VERTICAL POWER DMOSFETS IN SILICON CARBIDE

B. **Disclosure Date:** 12-19-04

C. Full legal names (including middle name) and titles of inventor/submitter(s) (Please print: Prof/Dr/Mr/Ms, followed by full legal name.

Title	Name	Phone No.	Department	Building
PROF.	JAMES A. (ALBERT) COOPER, JR	494-3514	ECE & BNC	EE
MS.	ASMITA SAHA	494-3706	ECE & BNC	EE

D. ***Disclosure must be reviewed and approved by Submitter's Department Head and Dean***

Department Head(s)	Signature	Date
MARK J.T. SMITH, ECE		01/03/05

Comments:

Dean(s) of School	Signature	Date
		01/07/05

Comments:

II. Sponsorship

Please specify the source of funds that were used in the research that led to the technology, including contract number from which salaries and other project costs were paid, which resulted in the disclosure. ***This information is critical for correct identification of sponsors and meeting obligations to them.***

A. **Government Agency/Address:** DARPA/MTO
3701 NORTH FAIRFAX DRIVE
ARLINGTON, VA 22203-1714

Contract/Grant #: N00014-03-1-0628
Grant/Contract Title: DEVELOPMENT OF PROCESS TECHNOLOGIES FOR HIGH-PERFORMANCE MOS-BASED SiC POWER SWITCHING DEVICES

B. **Name of department, industry, foundation or other sponsor/Address:**

Contract/Grant #:
Grant/Contract Title:

C. **Has the invention been disclosed to industry representatives? If "yes" please provide details, including names of companies and their representatives and dates:** NO

III. Publications, Public Use and Sale

Please be as thorough as possible, giving the *exact date and place* each event occurred. ***Valid patent protection depends on accurate answers to the following items.***

A. Dates, Places of the invention, and other pertinent data:
1. **Conception:** JAN - APRIL 2004
2. **First Sketch or Drawing:** APRIL 21, 2004
3. **First Written Description:** APRIL 21, 2004
4. **Model or Full Size Device, if any:** NONE YET
5. **First Test or Operation, if any:** NONE YET
6. **First Public Disclosure (and circumstances); Public disclosure is defined as oral or written information made availabl to the public in such a manner that said information can be understood by one skilled in the art:** NONE YET

B. Has proposed invention been disclosed in an abstract, paper, talk, news story or thesis? If "yes," please enclose drafts, abstracts, preprints.
Type of disclosure: NO **Disclosure Date:**

C. Is a publication, poster, thesis or other disclosure planned? When? If "yes," please enclose drafts, abstracts, preprints.
Type of disclosure: YES **Anticipated Date:** THESIS: SEPT. 2005

D. Has there been any public use or sale of products embodying the proposed invention? If yes, please describe, giving dates.
Description: NO **Date:**

E. Are you aware of related developments by others? If "yes," please give citations. Copies of any relevant Patents/Publications would be appreciated.
Citations: YES: OUR OWN WORK HAS LAID THE GROUNDWORK FOR THIS INVENTION, ONE EARLIER PATENT APPLICATION AND PUBLICATION.

F. List any closely related publications, patents, or patent applications of others which are known to you.
Publication/Patent Information: PURDUE PATENT APPLICATION: P-01104.00 (4-9-04 FILING)
PUBLICATION: M. MATIN, A. SAHA, & J.A. COOPER, IEEE TRANS. ON ELECTRON DEVICES, VOL. 51, PP. 1721-1725 (2004)

G. Do you currently have plans to make the disclosed material available to others? (YES) NO
If YES, please briefly describe the procedures you would follow to accomplish this:
THIS WORK WILL BE PRESENTED AT DARPA PROGRAM REVIEWS

IV. Detailed Description of the Invention

Please attach a detailed description of the invention. This description can be in the form of a manuscript, publication(s) or other written documents. This description *should* allow one skilled in the art to practice the proposed invention.

SEE PP. 51-52 OF PATENT NOTEBOOK (ATTACHED)
SEE ALSO: PHD THESIS PROPOSAL OF ASMITA SAHA, SCHOOL OF ELECTRICAL AND COMPUTER ENGINEERING, JULY 17, 2004.

V. Witness and Understand the Detailed Description of the Invention Disclosure

The undersigned witnesses have read and understood the detailed description for the above described invention disclosure.

SEE P. 52 OF PATENT NOTEBOOK (ATTACHED)

Witness Signature	Typed/Printed Name	Date
Witness Signature	Typed/Printed Name	Date

VI. Disposition of Royalties and Attestation

Each inventor should sign the *attestation* and indicate the agreed upon percentage of the inventor's share which should be awarded to each inventor.

The undersigned hereby attest(s) that the foregoing information is true and accurate.

I (We) agree with the provisions of Executive Memorandum B-10 and Business Office Memorandum 170. I (We) specifically recognize that the Committee on Patents and Copyrights shall as a general principle, but subject to all relevant provisions of Executive Memorandum B-10, award a two-third interest to the University and a one-third interest to the inventor/submitter(s) or creator(s) of the net proceeds derived from Inventions and Materials belonging to the University. I (We) hereby agree to divide said one-third interest in the proportions hereinafter specified before each signature below.

%	Signature (Inventor/Submitter)	Date
50	James A Cooper	12-19-04
50	Asmita Saha.	12-20-04
%	Signature (Inventor/Submitter)	Date
%	Signature (Inventor/Submitter)	Date

Please Note: If this disclosure is sent to a patent attorney for review, copies of the following information <u>may be required</u>:

1. **Copy of references**
2. **Copy of early notebook pages**
3. **Copy of first written description of proposed invention**
4. **Copy of first test/operation of proposed invention**

VII. Marketing Information

Please complete the following section thoroughly. Provide as much information as possible as it will be used to assess commercial potential and provide information to potential licensees.

A. **Disclosure Title:** OPTIMIZED VERTICAL POWER DMOSFETS IN SILICON CARBIDE

B. **Description of Invention (Please emphasize the benefits of the invention)**

C. **Why is this technology better than present technology?**

D. **What are its novel and unusual features?**

E. **What problems does the technology solve?**

F. **How were those problems solved in the past?**

SEE PP. 51-52 (ATTACHED)

G. **What company or companies are interested in the technology or are the major supplier(s) of similar technology**

CREE, INC.
NORTHROP-GRUMMAN
ROCKWELL
GENERAL ELECTRIC

H. **Describe briefly what will be required to complete the development of the invention before commercialization. Estimated Cost:** DEVICE FABRICATION IS UNDERWAY, AND DEMONSTRATION DEVICES SHOULD BE COMPLETED BY 30 JUNE 2005. WORK IS FUNDED BY DARPA/MTO.

VIII. Marketing Summary of the Invention (Non-confidential/Non-Technical Information)

Please summarize the invention in terms such that its value can be understood by a potential licensee. This summary will be used for distribution to companies to determine commercial interest in the proposed invention. Please provide a one *paragraph* concise description. This summary *must not* allow one skilled in the art to practice the proposed invention.

a structure and method of fabrication of vertical DMOS power transistors in silicon carbide to achieve close to the minimum theoretical on-state resistance at a given blocking voltage.

IX. Technology Classification

Please classify the disclosed technology in as many of the following areas that you believe apply to the technology.

LIFE SCIENCE / BIOTECHNOLOGY

- [ ] Animals
- [ ] Biomedical (Specify)
  - [ ] Diagnostic
  - [ ] Therapeutic
- [ ] Dental
- [ ] Foods and Nutrition
- [ ] Health Sciences
- [ ] Medical Devices (Specify)
  - [ ] Diagnostic
  - [ ] Therapeutic
- [ ] Pharmaceutical (Specify)
  - [ ] Diagnostic
  - [ ] Therapeutic
- [ ] Plants
- [ ] Other (Specify)

PHYSICAL SCIENCE

- [ ] Automotive Engineering
- [ ] Chemical Science/Chemical Engineering
- [ ] Construction, related
- [x] Electronics
- [ ] Energy
- [ ] Fluid Mechanics
- [ ] Manufacturing
- [ ] Materials
- [ ] Mechanical Engineering/Devices
- [ ] Separations
- [ ] Transportation
- [ ] Waste Treatment
- [ ] Other (Specify)

INFORMATION SCIENCE

- [ ] Computer Hardware (Specify)
  - [ ] Mainframe
  - [ ] UNIX
  - [ ] PC
- [ ] Computer Software
- [ ] Telecommunications
- [ ] Other (Specify)

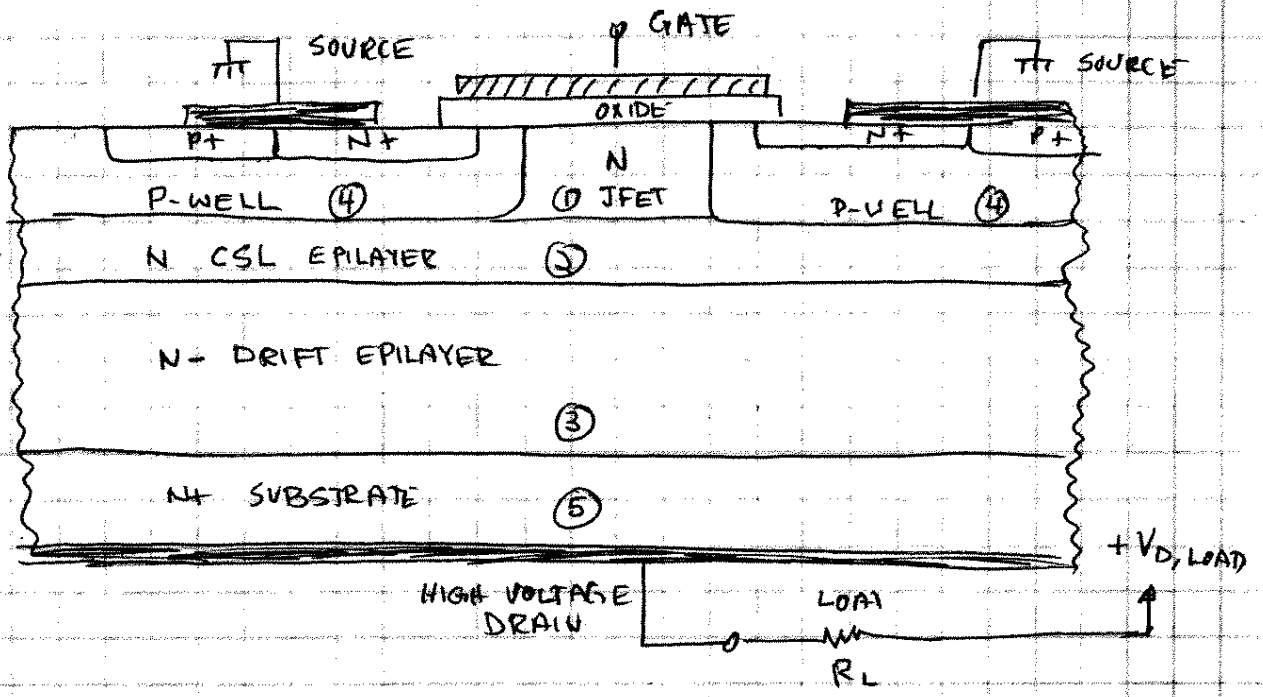
EDUCATIONAL MATERIAL

- [ ] Printed and/or Artwork Material
- [ ] Software
- [ ] Videos
- [ ] Multimedia
- [ ] Other (Specify)

OTHER (Specify)

Optimized Vertical Power DMOSFETs in SiC

Asmita Saha and I jointly developed the concept for optimized vertical power DMOSFETs that employ separately-doped JFET regions ① and lateral buried current spreading layers (CSL's) ② to achieve minimum on-resistance, as illustrated below...



Novel features of this invention are the CSL ②, which facilitate lateral current spreading under the p-wells in the ON state (reducing the overall device resistance) and the separately-doped JFET region ①, whose doping may be advantageously chosen to be higher than the doping of the N- drift layer ③ (to reduce the JFET

(continued next page)

resistance. These ideas are further described, and a detailed design optimization study is presented in the PhD proposal currently being written by A. Saha. Calculations and computer simulations indicate that a reduction on the order of 2-3x may be possible in the overall on-resistance of the device using these new features, <u>without</u> reducing the blocking voltage. The only changes to the fabrication sequence is that epilayers ① and ② would be ordered on the original wafer in addition to the usual epilayer ③.

Note that this structure can also be fabricated using the self-aligned procedure described on pp. 38-43 of this notebook, so as to achieve the lowest possible ON resistance.

Read and Understood Pages 51-52

Xiaokun Wang

April 26, 2004

James A. Cooper

April 26, 2004